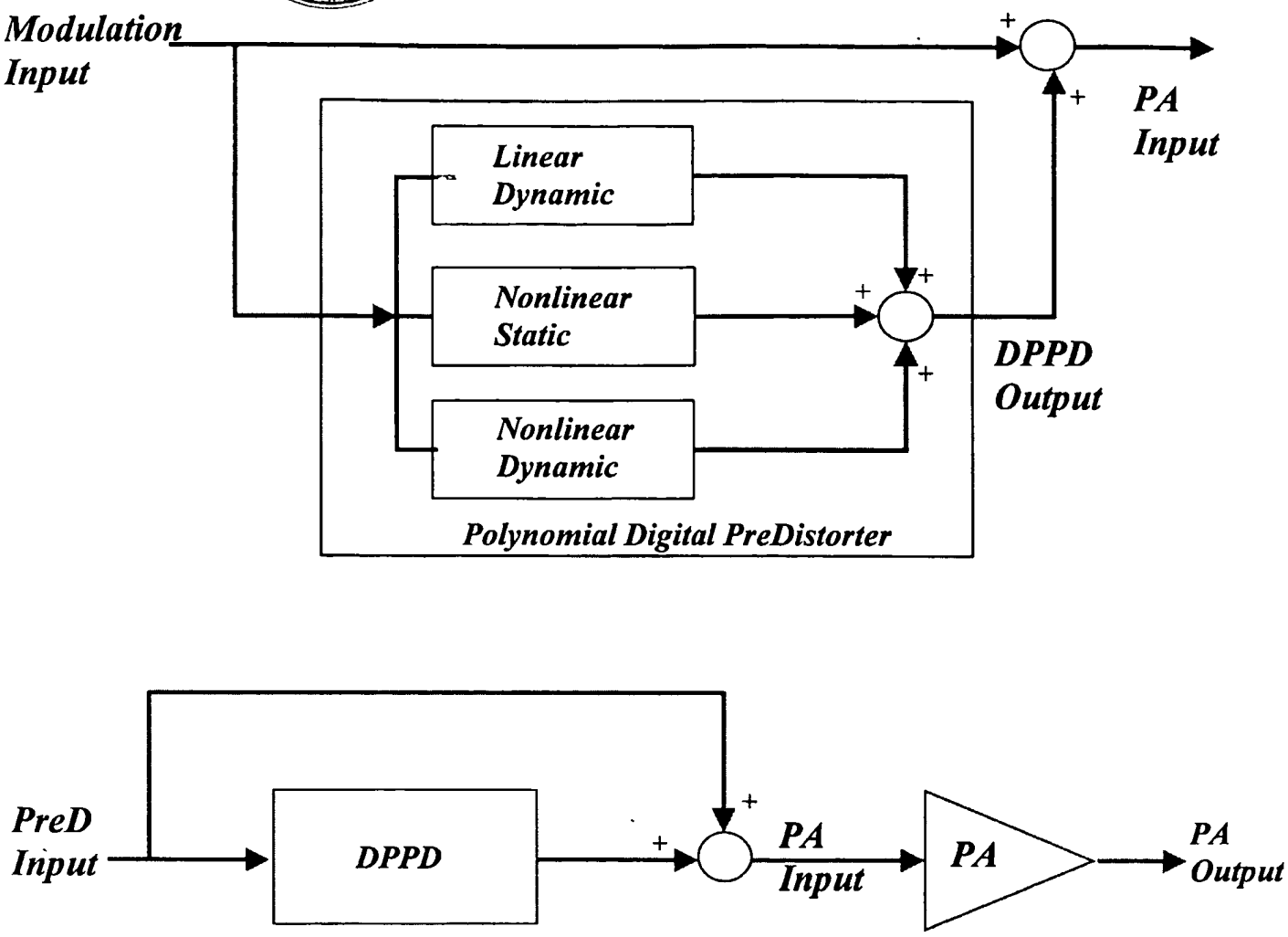

FIGURE 1 Functional block diagram of the additive polynomial predistorter

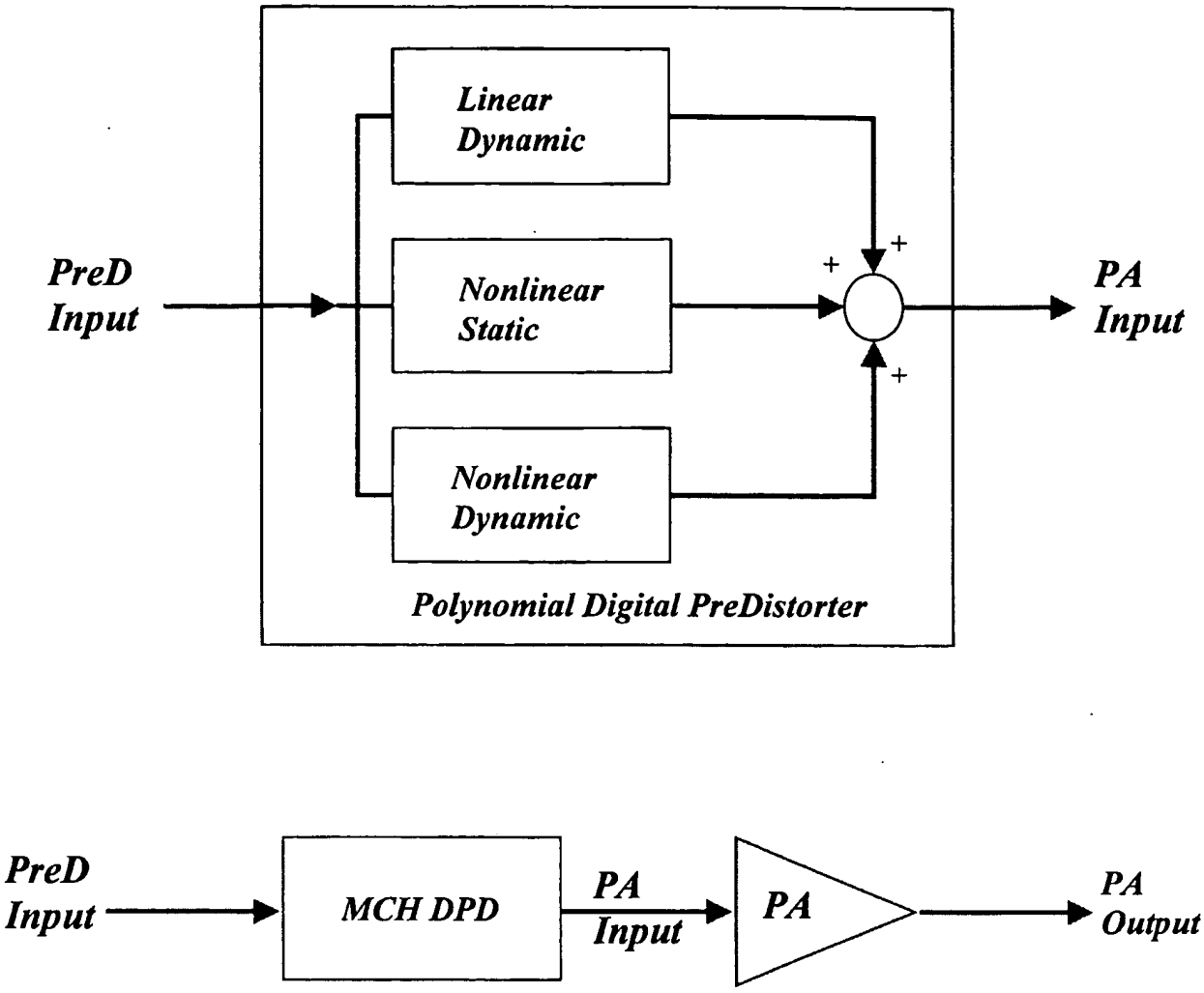

FIGURE 2 Functional block diagram of the multiplicative polynomial predistorter

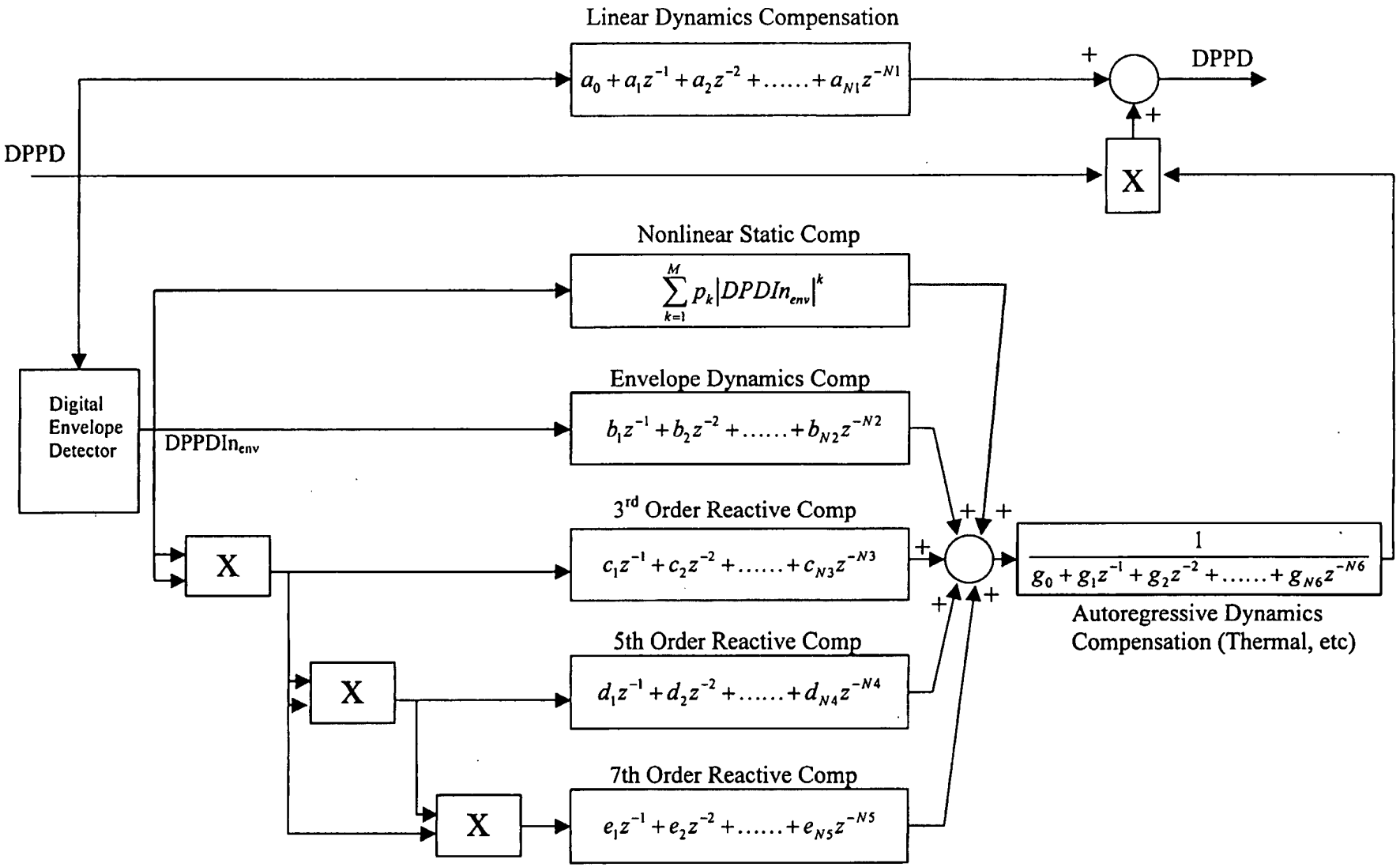

FIGURE 3 Block diagram of the polynomial predistorter of this invention

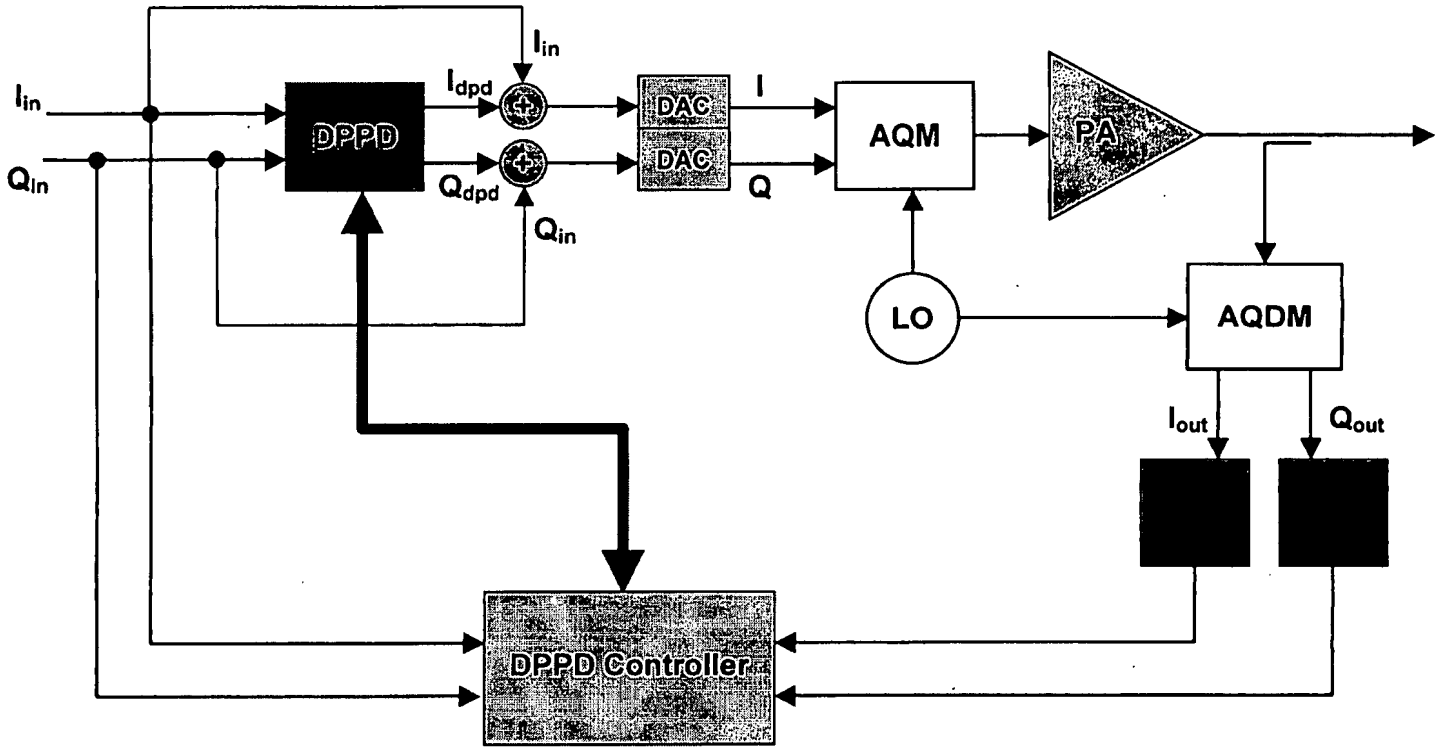

FIGURE 4 Block diagram of a predistortion system using this invention that employs an additive predistortion architecture

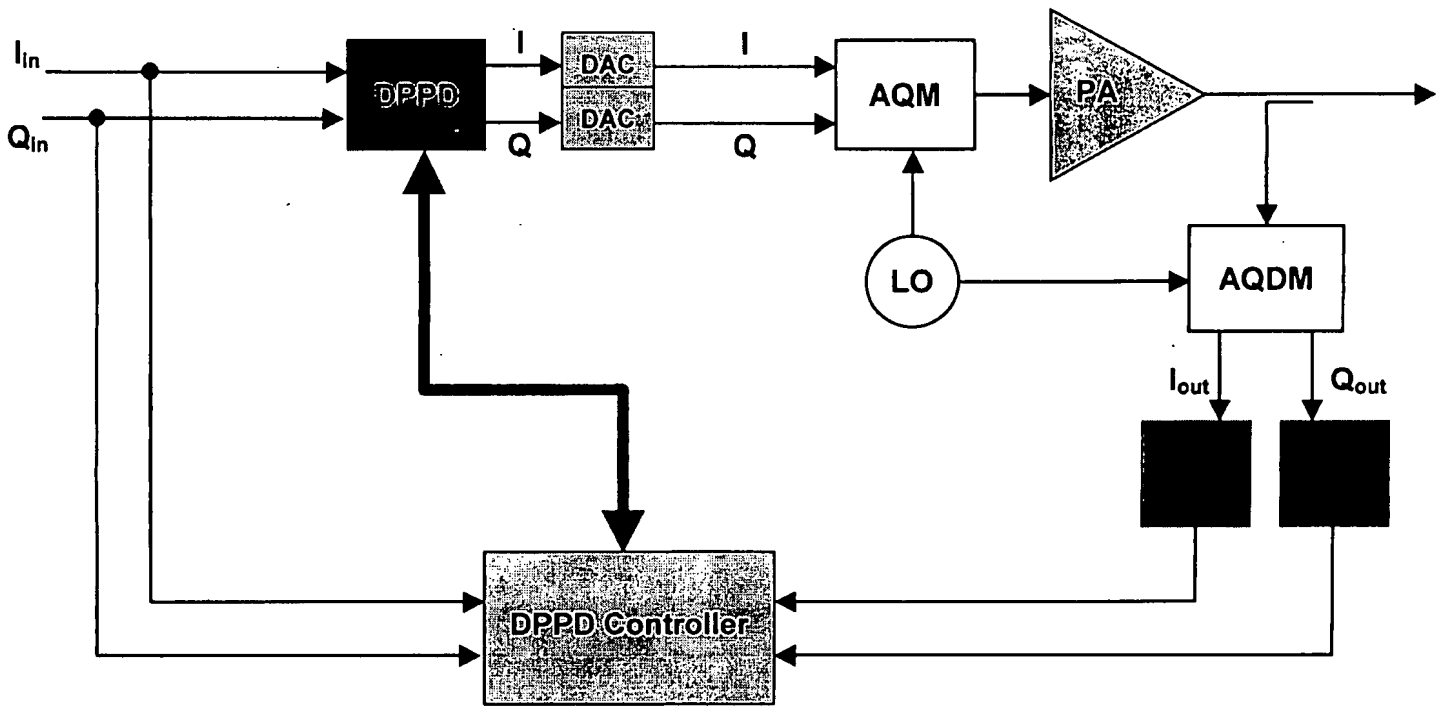

FIGURE 5 Block diagram of a predistortion system using this invention that employs a multiplicative predistortion architecture

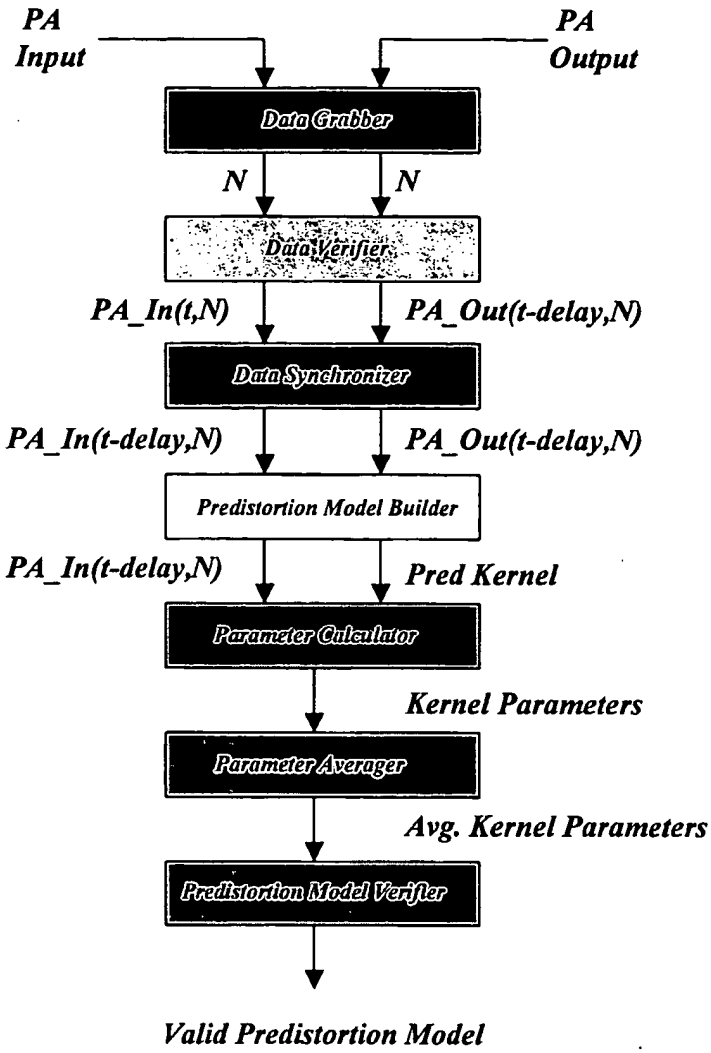

FIGURE 6 Flow chart diagram of the predistortion adaptation algorithm implemented in the DPPD controller